IN THE SPECIFICATION

Please amend the specification as follows:

Please replace paragraph [0001] with the following rewritten paragraph:

[0001] This application is a division of co-pending U.S. Patent Application Serial No. 09/970,758 entitled "Method For Fabricating A Power Semiconductor Device Having A Voltage Sustaining Layer With A Terraced Trench Facilitating Formation Of Floating Islands" filed on October 4, 2001 ~~This application is related to co-pending U.S. Application Serial No. 09/970,972 entitled "Method for Fabricating a Power Semiconductor Device Having a Floating Island Voltage Sustaining Layer," filed in the United States Patent and Trademark Office on October 4, 2001~~.

Please replace paragraph [0016] with the following rewritten paragraph:

[0016] FIG. 4 shows a power semiconductor device having floating islands of the type disclosed in co-pending U.S. Appl. Serial No. ~~[GS-158]~~ 09/970,972. In this device the trenches are assumed to be circular and therefore the floating islands are depicted as donut-shaped. Of course, the trenches may have other shapes such squares, rectangles, hexagons, or the like, which in turn will determine the shape of the floating islands. An N-type epitaxial silicon layer 401 formed over an N+ silicon substrate 402 contains P-body regions 405, and N+ source regions 407 for two MOSFET cells in the device. As shown, P-body regions 405a may also include deep P-body regions 405b. A source-body electrode 412 extends across certain surface portions of epitaxial layer 401 to contact the source and body regions. The N-type drain for both cells is formed by the portion of N-epitaxial layer 401 extending to the upper semiconductor surface. A drain electrode is provided at the bottom of N+ substrate 402. An insulated gate electrode 418 comprising oxide and polysilicon layers lies over the channel and drain portions of the body. A series of floating islands 410 are located in the voltage sustaining region of the device defined by epitaxial silicon layer 401. The floating islands are arranged in an array when

viewed from the top of the device. For instance, in FIG. 4, in the "y" direction, floating islands are denoted by reference numerals 410_{11}, 410_{12}, 410_{13}, ... 410_{1m} and in the "z" direction floating islands are denoted by reference numerals 410_{11}, 410_{21}, 410_{31}, ... 410_{m1}. While the column of floating islands 410 located below the gate 418 may or may not be employed, they are preferably employed when required for the device geometry and the resistivity of epitaxial layer 401.

Please replace paragraph [0020] with the following rewritten paragraph:

[0020] First, the N-type doped epitaxial layer 501 is grown on a conventionally N+ doped substrate 502. Epitaxial layer ~~1~~ 501 is typically 15-50 microns in thickness for a 400-800 V device with a resistivity of 5-40 ohm-cm. Next, a dielectric masking layer is formed by covering the surface of epitaxial layer 501 with a dielectric layer, which is then conventionally exposed and patterned to leave a mask portion that defines the location of the trench 520_1. The trench 520_1 is dry etched through the mask openings by reactive ion etching to an initial depth that may range from 5-15 microns. In particular, if "x" is the number of equally spaced horizontal rows of floating islands that are desired, the trench 520 should be initially etched to a depth of approximately 1/(x+1) of the thickness of the portion of epitaxial layer 502 that is between the subsequently-formed bottom of the body region and the top of the N+ doped substrate. The sidewalls of each trench may be smoothed, if needed. First, a dry chemical etch may be used to remove a thin layer of oxide (typically about 500 – 1000 A) from the trench sidewalls to eliminate damage caused by the reactive ion etching process. Next, a sacrificial silicon dioxide layer is grown over the trench 520_1. The sacrificial layer is removed either by a buffer oxide etch or an HF etch so that the resulting trench sidewalls are as smooth as possible.

Please replace paragraph [0023] with the following rewritten paragraph:

[0023] Next, in FIG. 5(d), a third trench 520_3 (most clearly seen in FIGS. ~~3(e)~~ 5(e) and ~~3(f)~~ 5(f)) may be formed by first growing an oxide layer 524_2 on the walls of trench 520_2. Once again, the thickness of the silicon dioxide layer 524_2 will determine the differential in

diameter (and hence the radial width of the resulting annular ledge) between trench 520_2 and trench 520_3. Oxide layer 524_2 is removed from the bottom of the trench 520_2. This process can be repeated as many times as necessary to form the desired number of trenches, which in turn dictates the number of annular ledges that are to be formed. For example, in FIG. 5(d), four trenches 520_1-520_4 (more clearly seen in FIG. ~~3(e)~~ 5(e)) are formed.

Please replace paragraph [0025] with the following rewritten paragraph:

[0025] The diameter of trenches ~~520_1-5204~~ 520_1-520_4 should be selected so that the resulting annular ledges 546_1-546_3 and the trench bottom all have the same surface area. In this way, when a dopant is introduced into the ledges and trench bottom, each resulting horizontal plane of floating islands will have the same total charge.